Performance Comparison of 5GHz VCOs Integrated by CMOS Compatible High Q MEMS Inductors

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Abstract — **In this paper we report the performance comparison of 5GHz CMOS VCOs fabricated by 0.18μm six-metal mixed-mode RF CMOS processes with respect to the same VCOs integrated with high Q MEMS inductors. The CMOS inductors implemented by a top-level 2μm-thick Al/Cu metal layer typically show Q factors of about 10, while the MEMS inductors can give much higher Q factors over 25. Differential CMOS VCO circuits have been optimally designed for the respective Q factors of both CMOS and MEMS inductors. Phase noise has been measured and compared for the fabricated VCOs, demonstrating that the VCOs with MEMS inductors can give better phase noise by more than 7dB in the offset frequency range from 30kHz to 3MHz.**

I. INTRODUCTION

Voltage controlled oscillator (VCO) is one of challenging components for RF circuit design engineers. Although significant amount of research work has been carried out on VCOs, there still remains room for improvement and many new circuit schemes and new interpretation of phase noise can be found in recent literatures [1-6]. One effort is to push oscillation frequencies up to the upper limit that current process technologies can provide. There used to be a race to increase the oscillation frequencies in a simple VCO circuit architecture for the last decade. The other effort is to improve phase noise at a given oscillation frequency. The effort is motivated by more stringent requirements imposed on VCO design in wireless communications applications at higher frequencies. Recently, new circuit schemes have been reported to improve phase noise including transformer-coupled VCO [7], differential Colpitts VCO [8], and distributed VCO using transmission lines [9]. Most of the recent attempts have used the on-chip passive components available from the existing process technologies, which typically have poor performance due to large ohmic loss resulting from thin metal layers and substrate loss resulting from conductive silicon substrate.

Most of endeavors to improve phase noise have been limited to circuit techniques using conventional standard process technologies and have met difficulty in substantially improving it in the device level. It is often found that the integrated VCOs using standard silicon processes have hard time to meet rigorous communication specifications with enough margin due to their relatively poor characteristics of available passive components such as on-chip inductors. Phase noise, one of the major specifications in VCOs, is directly related with quality factor (Q) of an LC resonator used in VCO circuits. Generally, the inductors obtained from standard silicon processes cannot provide sufficient Q factors. (Typical Q factors from commercially available silicon processes are less than 12 in 1~5 GHz range.) Therefore, it is required to devise a new way of providing integrated high Q on-chip inductors in order to intrinsically improve the performance of VCOs. Recently, there are a few attempts to integrate MEMS inductors for RF circuit applications [10-13].

In this paper, we report the performance comparison of 5 GHz VCOs with or without using MEMS inductors, realized in 0.18 μm mixed-mode RF CMOS processes. We have designed CMOS VCOs using standard processes with the top layer metal for inductors. We have also implemented MEMS VCOs for low phase-noise by monolithically integrating MEMS inductors with a higher Q factor over 25. We have observed the performance improvement in MEMS VCOs by more than 7 dB in various offset frequencies. Design issues, fabrication and measured performance comparison of both VCOs with or without MEMS inductors will be reported in the following sections.

II. VCO CIRCUIT DESIGN

Figure 1 shows the CMOS cross-coupled differential VCO circuit schematic used for our performance comparison study. This scheme has been chosen because it is one of typical differential VCO circuits which can give large signal swings as well as generate symmetric signals [14]. Oscillation frequency is determined by the inductance and capacitance values in the LC tank. For CMOS VCOs, a top metal layer (2 μm-thick Al/Cu) has been used for inductors.

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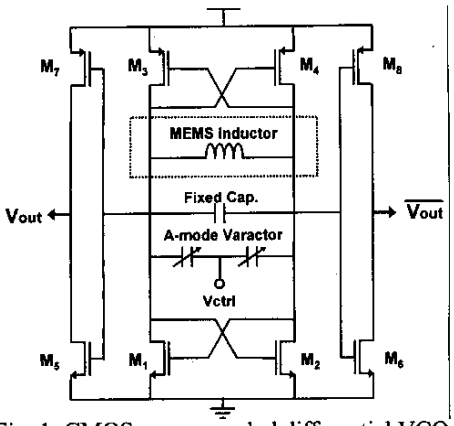

Fig. 1. CMOS cross-coupled differential VCO.

As for MEMS VCOs, the top metal layer inductor is replaced by MEMS inductors as shown in Fig. 2. These suspended MEMS inductors are integrated on the top of the CMOS core circuit by using surface micromachining technology. The detailed implementation processes can be found elsewhere [15]. Both inductors have been designed for their Qs to be maximum at the operating frequency of 5 GHz. For inductor layout, a simulation program, Momentum, has been used for their optimization. The capacitance in the LC tank should be selected to provide its Q peak much higher than that of inductors by at least a factor of two in order to ensure the total resonant Q of the LC tank would not be affected by poor capacitance Q factors. In this implementation, the capacitance consists of two capacitors: an accumulation-mode MOSFET varactor for frequency tuning and a fixed capacitor for higher Q factor. The MOSFET varactor is known to have high Q and relatively large tuning range [16]. The total tuning range has been designed to be about 20%.

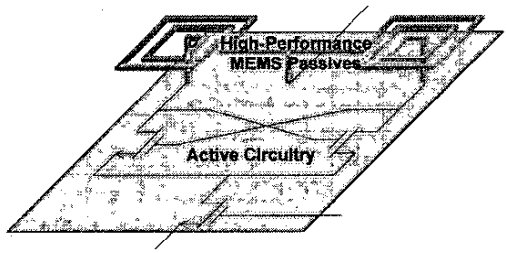

Fig. 2. Concept of VCOs with integrated on-chip MEMS inductors.

Core active components consist of four transistors (M_1~M_4) which compensate for the loss in the LC tank. Other transistors (M_5~M_8) are used as buffer stages to isolate the LC tank from the 50Ω termination of spectrum analyzer and to generate 0dBm output power. In this scheme, current source is not employed in order to maximize signal swings and minimize any noise generated in the additional active devices. The output is measured via DC blocking capacitor embedded in the circuit. No external components have been used for matching.

Circuit simulation has been conducted by Agilent ADS simulation tool. In circuit implementation, a 0.18 μm mixed-mode 6-metal CMOS process has been used. Inductance and capacitance of the LC tank has been determined as 1nH and 1pF, respectively, for 5 GHz operation. Actually, the capacitance is composed of two parts: a fixed capacitor of 0.4pF and a variable capacitor of 0.2~0.6pF for tuning. The variable capacitor is realized by an accumulation-mode MOSFET varactor. Active devices optimization procedure has been conducted in two steps: the ratio of nMOS and pMOS is optimized for flicker noise reduction; and the actual nMOS width optimized for thermal noise reduction. From the simulation results, the optimal ratio of nMOS and pMOS has been obtained as 1:2.5. The result approximately agreed with the inverse ratio of nMOS and pMOS mobility. After determining transistor ratio, the final width of nMOS has been optimized as 20 μm (with 8 μm width legging) for the given Q factor.

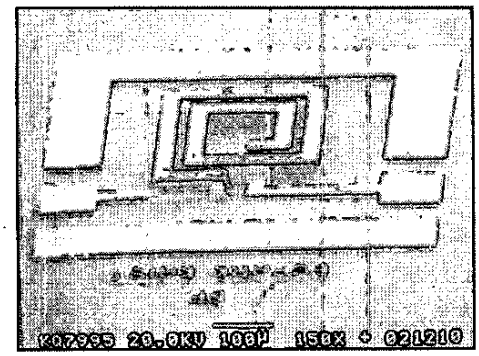

Fig. 3. Measurement pattern for 1 nH MEMS inductor.

III. MEMS INDUCTOR

Figure 3 shows fabricated MEMS inductors using surface micromachining on a silicon test wafer. The test wafer has 1 μm thick oxide on the top of the substrate silicon (10 Ω-cm) for electrical isolation. Main body of MEMS inductors is suspended from the substrate by 25 μm. The outer dimension of the inductor is 310 μm, and the line/space are 30/20 μm, respectively. To characterize the fabricated inductors, on-wafer RF measurement has been performed from 0.5 GHz to 10 GHz using HP8720 network analyzer. The maximum Q of the MEMS inductor is higher than 25 at operating frequency regions as shown in Figure 4.

III. INTEGRATED MEMS VCOS

Figure 5 shows the integrated MEMS VCO. A MEMS inductor has been integrated on the top of active circuits realized using a 0.18 μm CMOS process. As post CMOS

processes, special surface micromachining processes have been developed to provide a monolithic solution for high Q inductors by using conventional lithography and electroplating processes. Basically, thick photoresist lithography frequently used in MEMS applications is employed to form an electroplating mold as well as a sacrificial layer. Then, copper electroplating follows to fill the patterned photoresist mold. Finally, photoresist is removed.

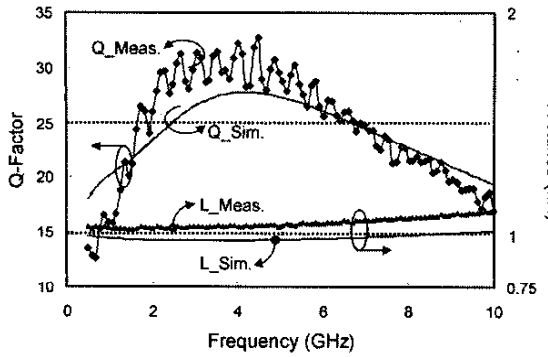

Fig. 4. Characteristics of 1nH MEMS inductor

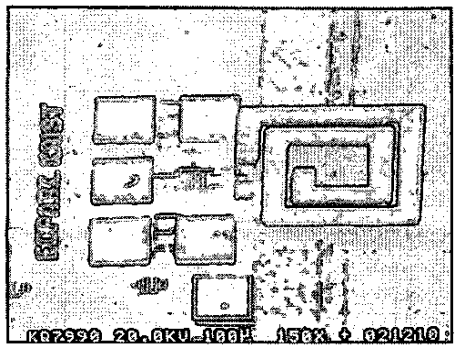

Fig. 5. Fully integrated 5 GHz CMOS VCO with an MEMS inductor.

Detailed process flows are explained in the following [15]. Fabrication starts with a wafer on which CMOS active devices as well as interconnection metals and top insulation layer with pad openings have been completed (Fig. 6-a). Ti/Cu (20/100 nm) is thermally evaporated as a seed layer for electroplating. Thick photoresist (AZ9260, about 10 μm) is spun and patterned to form electroplating molds. Cu is electroplated through the mold to form bottom electrodes (Fig. 6-b). Second thick photoresist (about 30 μm) is spun on the wafer followed by the two-step UV exposure using two different photomasks at different exposure times. A 3-D photoresist mold is formed by single-step development (Fig. 6-c). The thickness of the developed photoresist is well controlled by UV expose time [15]. The lower recessed region (about 15 μm) is filled with the electroplated Cu to form the posts (Fig. 6-d). After the post electroplating, second seed metal (Cu) is deposited by thermal evaporation on the wafer (Fig. 6-e). The topmost seed metal is removed in order to confine the electroplating of Cu only in the upper recessed region (Fig. 6-f). The dashed line shown in Fig. 6-e indicates the boundary to which the mechanical polishing is done. Then, Cu is electroplated from the bottom of upper recessed region (Fig. 5-g). Finally, suspended MEMS structures are completed by removal of photoresist and seed layers (Fig. 5-h).

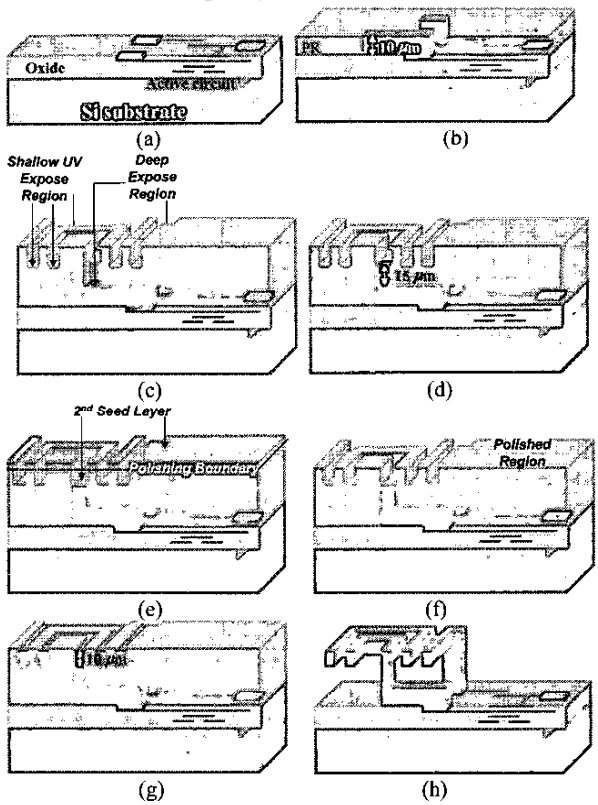

Fig. 6. MEMS inductor integration process

III. Measurement Results

Phase noise has been measured for MEMS VCOs using an HP8564E spectrum analyzer at the oscillation frequency of 5 GHz and shown in Figure 7. Phase noise of −122 dBc/Hz has been achieved at 1 MHz offset from 5 GHz center frequency. The VCO tuning range has been measured by varying the control voltage of the varactor from 0 to 2 V. Oscillation frequency has been tuned from 4.7 GHz to 5.6 GHz (about 20%) with constant output power of 0 dBm. Figure 8 shows the measured tuning characteristics. The fabricated MEMS VCO consumes 3.75mW from a 1.5 V power supply in the VCO core and its size is 0.22 mm^2.

CMOS VCOs have been characterized in the same manner. All the characteristics including output power,

tuning range and power consumption show similar to the MEMS VCOs except for phase noise. Phase noise in CMOS VCOs are higher by more than 7dB compared to the MEMS counterparts. Figure 9 shows the phase noise difference between MEMS and CMOS VCOs. MEMS VCOs show better noise performance by more than 7dB in various offset frequencies at different control voltages of the MOSFET varactor.

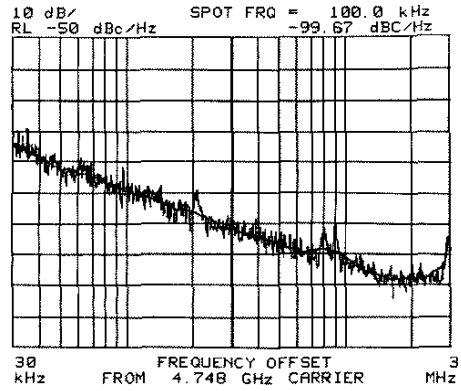

Fig. 7. Phase noise plot of 5 GHz MEMS VCO.

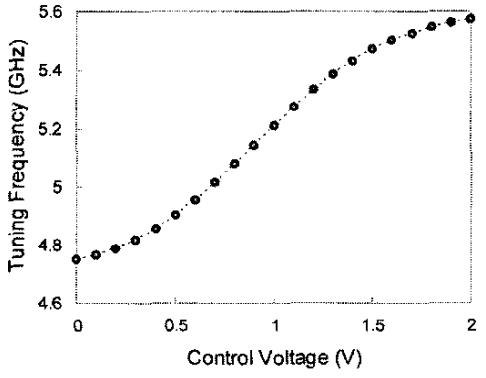

Fig. 8. Tuning characteristics of 5 GHz MEMS VCO.

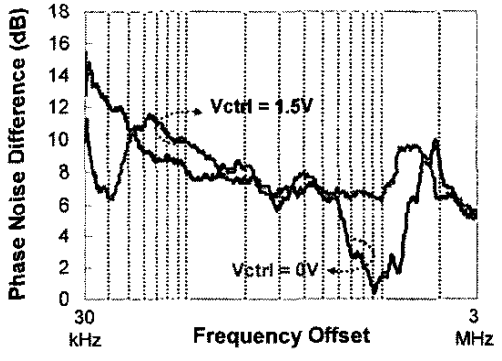

Fig. 9. Phase noise improvement of MEMS VCO to CMOS VCO for different offset frequencies.

III. Conclusions

We have designed and fabricated a 5GHz low phase noise MEMS VCO by monolithically integrating suspended MEMS inductors on the top of the cross-coupled differential VCO core circuits realized by 0.18 μm six-metal mixed-mode RF CMOS processes. Phase noise has been compared with CMOS VCOs in which inductors are implemented by a top-level 2 μm-thick Al/Cu metal layer. It has been demonstrated that MEMS inductors can improve phase noise by more than 7dB due to their high Q factors.

Acknowledgements

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References

[1] B. Razavi, "A Study of Phase Noise in CMOS Oscillators," *IEEE J. Solid-State Circuits*, vol. 31, No. 3, pp. 331-343, Sep. 1996.

[2] J. Craninckx, M. Steyaert, and H. Miyakawa, "A Fully Integrated Spiral-LC CMOS VCO Set with Prescaler for GSM and DCS-1800 Systems," *Custom Integrated Circuits Conference*, 1997, pp. 403-406.

[3] A. Hajimiri, and T. Lee, "A General Theory of Phase Noise in Electrical Oscillators," *IEEE J. Solid-State Circuits*, vol. 33, No. 2, pp. 179-194, Feb. 1998.

[4] F. Herzel, M. Pierschel, P. Weger, and M. Tiebout, "Phase Noise in a Differential CMOS Voltage-Controlled Oscillator for RF Applications," *IEEE tr. Circuits and Systems*, vol. 47, No. 1, pp. 11-15, Jan. 2000.

[5] J. Rael, and A. Abidi, "Physical processes of Phase Noise in Differential LC Oscillators," *Custom Integrated Circuits Conference*, pp.569-572, 2000.

[6] D. Ham, and A. Hajimiri, "Concepts and Methods in Optimization of Integrated LC VCOs," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 6, June 2001.

[7] M. Straayer, et al., "A Low-Noise Transformer-Based 1.7 GHz CMOS VCO," *IEEE ISSCC Digest of Technical Papers*, pp. 286-287, 2002.

[8] R. Aparicio, A. Hajimiri, "A noise-shifting differential colpitts vco," Solid-State Circuits, *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 1728 -1736, 2002.

[9] B. Kleveland, et. al., "Exploiting CMOS Reverse Interconnnect Scaling in Multigigahertz Amplifier and Osicllator Design," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 1480-1488, no. 10, 2001.

[10] J. Roger, et. al., "Post-Processed Cu Inductors with Application to a Completely Integrated 2-GHz VCO," *IEEE tr. Electron Devices*, vol. 48, pp.1284-1287, 2001.

[11] Y. Chen, et. al., "A 2.4GHz Integrated CMOS Power Amplifier with Micromachined Inductors," *MTTs*, pp. 523-526, 2001.

[12] E.-C. Park, J.-B. Yoon, S. Hong, and E. Yoon, "A 2.6GHz Low Phase Noise VCO Monolithically Integrated with High-Q MEMS Inductors," *European Solid-State Circuit Conf.*, 2002, pp. 143-146.

[13] E.-C. Park, Y.-S. Choi, J.-B. Yoon, S. Hong, E. Yoon, "Fully Integrated Low Phase-Noise VCOs with On-Chip MEMS Inductors," *IEEE Trans. Microwave Theory Tech.*, vol. 51, no. 1, pp. 289-296, Jan. 2003.

[14] S. Levantino, et. al. "Frequency Dependence on Bias Current in 5-GHz CMOS VCOs: Impact on Tuning Range and Flicker Noise Upconversion," *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 1003-1011, Aug. 2002.

[15] J.-B. Yoon, B.-I. Kim, Y.-S. Choi, and E. Yoon, "3-D Lithgraphy and Metal Surface Micromachining for RF and Microwave MEMS," *MEMS'02*, pp. 673-676.

[16] F. Svelto, S. Deantoni, and R. Castello, "A 1.3 GHz Low-Phase Noise Fully Tunable CMOS LC VCO," *IEEE J. Solid-State Circuits*, vol. 35, No. 3, pp. 356-361, Mar. 2000.